

CLAIMS

1. A semiconductor device comprising:
 - a substrate;
 - a drain formed in the substrate;
 - a self-aligned source formed in the substrate;
 - a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;
 - a first polysilicon deposited over the first oxide layer;
 - a second oxide layer deposited over the first polysilicon layer;
 - a second polysilicon layer deposited over the second oxide layer; and
 - a phosphorous-doped oxide along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer.
2. The semiconductor device of claim 1, wherein the first oxide layer is a tunnel oxide layer.
3. The semiconductor device of claim 1, wherein the second oxide layer is an oxide nitride oxide layer.
4. The semiconductor device of claim 1, wherein the first polysilicon layer is a floating gate.
5. The semiconductor device of claim 1, wherein the second polysilicon layer is a wordline.

6. A semiconductor device after re-oxidation comprising:

- a substrate;
- a drain formed in the substrate;
- a self-aligned source formed in the substrate;
- a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;
- a first polysilicon layer deposited over the first oxide layer;
- a second oxide layer deposited over the first polysilicon layer;
- a second polysilicon layer deposited over the second oxide layer;
- a phosphorous doped oxide layer along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer; and
- a re-oxidation oxide profile formed over surfaces of the semiconductor device having a height and width.

7. The device of claim 6, wherein the height is a vertical distance from the source to a bottom edge of the first polysilicon layer and the width is a horizontal distance from a side edge of the first polysilicon layer to a vertical edge of the tunnel oxide layer.

8. The device of claim 6, wherein the height and width are determined by characteristics of the phosphorous doped oxide.

9. A self aligned source of a flash memory device on a substrate, the self aligned source comprising:

one or more horizontal surfaces planar to the substrate having a desired doping concentration;

one or more vertical surfaces perpendicular and coupled to the one or more horizontal surfaces, the one or more vertical surfaces having a lower than desired doping concentration; and

one or more vertical phosphorous-doped oxide layers formed over the one or more vertical surfaces, the one or more vertical phosphorous-doped oxide layers having an additional doping concentration.

10. The self aligned source of claim 9, wherein the additional doping concentration and the less than desired doping concentration produce an effective doping concentration.

11. The self aligned source of claim 10, wherein the effective doping concentration is substantially equal to the desired doping concentration.

12. The self aligned source of claim 9, wherein the additional doping concentration, the less than desired doping concentration and the desired doping concentration are selected to provide a desired resistance.

13. A computer system comprising:
- at least one processor;
 - a system bus;
 - a flash memory device coupled to the system bus, the memory device including one or more flash memory cells comprising:
 - a substrate;
 - a drain formed in the substrate;
 - a self-aligned source formed in the substrate;
 - a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;
 - a first polysilicon deposited over the first oxide layer;
 - a second oxide layer deposited over the first polysilicon layer;
 - a second polysilicon layer deposited over the second oxide layer;
 - a phosphorous doped oxide along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer; and
 - a re-oxidation oxide profile formed over surfaces of the semiconductor device having a height and width.